**Boot camp for Digital Systems Education**

Using a low cost FPGA board for learning digital electronics

Sponsored by a grant from the IEEE Computer Society for Emerging Technology

Conducted over two Saturdays at St. Mary’s University room 111 Richter Math-Engineering building. Starting June 11 from 9AM to 4PM. Lunch will be provided. Those that complete the two sessions keep their FPGA board.

Open to College, pre-college, high school, junior college and continuing education students. Reservations at <https://events.vtools.ieee.org/m/316279> Necessary for a head count and to order FPGA boards. Students expected to have or share an x86 PC. Students expected to have some familiarity with binary arithmetic and Boolean logic

Day 1 (June 11):

Install Digital logic simulator on a PC

Install configuration files for FPGA board

FPGA board background

Logic simulator background

Example circuits

Draw logic circuits

Operate logic circuits

Generate RTL files for FPGA board

Examine RTL files

Repeat

Day 2 (June 18):

Install Xilinx Vivado on a PC

Vivado background

RTL background

Constraint file background

Initialize project

Load RTL and constraint files

Compile, place and route

Download to FPGA board

Exercise design

Repeat

At the end of day one student should be able to create and exercise a digital design of their choosing. At the end of day two the student should be able to exercise the digital design on the FPGA board. Proctors will be available to help with error messages, RTL syntax issues or other problems.

The purpose of the grant is to make FPGA education more available and affordable on a par with Raspberry Pi or Arduino. It is an experiment. The Boot Camp is the first cut at a beginning FPGA (AKA modern digital systems) education with student ownership of the FPGA board. There is much to learn. Afterwards the student is expected to make progress on their own or in a class. The RealDigital.org FPGA board web site has a 15 week course.

**Boot camp for Digital Systems Education (cont’d)**

Web links and instructions 1st Saturday

Digital simulator web site <https://github.com/hneemann/Digital/releases/> contains **Digital.zip** with the documentation files in the **docu** sub-directory. The base web page <https://github.com/hneemann/Digital> contains installation instructions and a comprehensive description (as well as the **download link**).

Unzip **Digital.zip** to a convenient location. The Digital directory should contain **Digital.exe** and **Digital.jar** files. You need to have Java installed. Double click one of the **exe** files to start the simulator. Do some of the exercises in the manual until you are comfortable with the tool.

The Digital schematic tool is completely interactive. First task should be to connect one or more switches to corresponding LEDs. Once this is working one can add logic gates with switch inputs and LED outputs. One should also wire up a free running counter to several LEDs. Select a frequency such that one of the counter bits toggle at a once a second and some other counter bits toggle more and less frequently.

Some basic circuits, in order of complexity, are: the full adder, multiplexer, Arithmetic Logic Unit, barrel shifter and Wallace tree multiplier (see Wikipedia entries, the entry for ALU has VHDL source code).

To target the RealDigital FPGA board one needs to insert a Booleanbd.config[[1]](#footnote-1) file into the **examples/hdl** sub-directoy. Then go down the menu tree **Edit**/**Settings**/ **Advanced** and select the file. A **Toolchain Configuration** file, **Booleanbd.config** also needs placed in the **examples/hdl** subdirectory. Select **Booleanbd.config**. This will add a menu entry of the same name that is used to write out the VHDL or Verilog source files to use with the Vivado tool (next Saturday). For today we merely want to examine the RTL and constraint files (***design-name*.v** or ***design-name*.vhdl** and ***design-name*\_constraints.xdc**) using your favorite language sensitive editor (I use **notepad++**).

1. To be found at the IEEE web page <https://events.vtools.ieee.org/m/316279> [↑](#footnote-ref-1)